ABSTRACT OF THE DISCLOSURE

This invention has as its object to suppress an increase in circuit scale and to simplify a circuit structure by executing a filter process using a plurality of arithmetic units each of which makes multiplication and addition.

To achieve this object, image data Y_{n+2}, Y_{n+3}, and Y_{n+4} to be processed are read out (S2901), and three lattice point data d'_{n+1}, S'_n, and d_{n-1} are respectively read out from sequences H1, H2, and H3 corresponding to line buffers that store the lattice point data (S2903). $d'_{n+3} = Y_{n+3} + \alpha \cdot (Y_{n+2} + Y_{n+4})$ is computed (S2905), and d'_{n+3} is stored in the sequence H1 (S2907). $S'_{n+2} + \beta \cdot (d'_{n+1} + d'_{n+3})$ is computed (S2909), and S'_{n+2} is stored in the sequence H2 (S2911). $d'_{n+1} = d'_{n+1} + \gamma \cdot (S'_{n+2} + S'_n)$ is computed (S2913), and d_{n+1} is stored in the sequence H3 (S2915). $S_n = S'_n + \delta \cdot (d_{n-1} + d_{n+1})$ is computed (S2917), and S_n and d_{n+1} are output to the next processing stage (S2919).